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# Origin of the Hysteresis in I-V Curves for Planar Structure Perovskite Solar Cells Rationalized with a Surface Boundary Induced Capacitance Model

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# Origin of the Hysteresis in I-V Curves for Planar Structure Perovskite Solar Cells Rationalized with a Surface Boundary Induced Capacitance Model

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For the efficient hybrid solar cells based on the organometal halide perovskites, real origin of the I-V hysteresis became a big issue and has been discussed widely. In this study, simulated I-V curves of different equivalent circuit models were validated with experimental I-V curves of a planar perovskite solar cell with the power conversion efficiency (PCE) of 18.0% and 8.8% on reverse scan (from open circuit to short circuit) and forward scan (from short circuit to open circuit) respectively. We found that an equivalent circuit model with a series of double diodes, capacitors, shunt resistances, and single series resistance produces the simulate I-V curves with large hysteresis matching with the experimentally observed curves. The electrical capacitances generated by defects due to the lattice mismatch at the $TiO_2$/$CH_3NH_3PbI_3$ and $CH_3NH_3PbI_3$/spiro-OMeTAD interface are truly responsible for the hysteresis in the perovskite solar cells.

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The perovskite solar cells based on $CH_3NH_3PbI_3$ have attracted enormous attention in the last few years due to the outstanding performance as the photovoltaics. The power conversion efficiency (PCE) of the devices has dramatically improved to over 20% in relatively short durration.[1,2] Despite the unique properties and higher efficiencies, several important issues, e.g. mysterious hysteresis in I-V curves and durability of stabilized performance, still remained for the commercialization.[3,4] It has been found the hysteresis strongly depends on the device architecture, where the planar structure and $Al_2O_3$ mesoscopic perovskite cells show relatively large hysteresis than $TiO_2$ mesoporous structure devices.[5] The typical planar of $SnO_2$:F(FTO) / compact $TiO_2$ / $CH_3NH_3PbI_3$/ spiro-OMeTAD / Au,[6] suffers from severe hysteresis in the I-V measurement.[3,4] The reverse scan (from the open circuit to the short circuit) always shows higher PCE than the forward scan (from short circuit to the open circuit). Hence, such hysteresis in the I-V curves creates ambiguity about the actual performance of the device, which is being suspected to be over-estimated.[7,8]

The origin of hysteresis has been discussed on the intrinsic proprieties like ferroelectric polarization[9] and/or ionic migration[10] of the perovskite to date. However, there was no direct evidence that could support the above claims. It has been reported that passivation of $TiO_2$ layer by C60 or use of phenyl-C61-butyric acid methyl ester (PCBM) instead of $TiO_2$ in inverted device structure reduces the hysteresis.[11-13] The passivation could minimize the trap states and improve electron transfer through the interface of $TiO_2$/$CH_3NH_3PbI_3$, resulting in reduction of hysteresis.[11] On the other hand, PCBM in the inverted cell could extract the carriers (electrons) more efficiently than $TiO_2$ without accumulation at the interface, and the hysteresis was eliminated. In another standpoint, lattice mismatch of the interfaces containing organic compounds could be ignored and consequently the hysteresis was reduced. The importance of lattice mismatch is widely known and discussed for inorganic thin film solar cells.[14] Due to the higher expansion coefficient of $CH_3NH_3PbI_3$ than $TiO_2$, an interfacial stress is created at the interface of $TiO_2$ / $CH_3NH_3PbI_3$ which changes with temperature.[15,16] The above reports strongly suggest that defects and/or traps at the interface between compact $TiO_2$ and $CH_3NH_3PbI_3$ play an important role in causing the hysteresis. The charge trapping / detrapping and/or charge accumulation caused by the lattice mismatch or voids at this interface act as *capacitors*. In the present study, we confirm "a double diode equivalent circuit model" including the interfacial capacitive components where the hysteresis essentially comes up due to carrier accumulation at the interfaces.

For the model study, we used high efficiency planar perovskite solar cells showing large hysteresis in the I-V curves. The planar structured perovskite solar cells using $TiO_2$ substrate coated on flat FTO substrate (SPD laboratory, sheet resistance 7 Ω/square, average transmittance in visible range 81%, FTO thickness 800 nm) were fabricated by one-step solution deposition method. $CH_3NH_3PbI_3$ was prepared using mixed halide precursors ($PbCl_2$ and $CH_3NH_3I$) dissolved in dimethylformamide (DMF), as described previously.[17-19] Spiro-OMeTAD was used as p-type hole extracting layer. Finally, gold back contact layer was deposited on spiro-OMeTAD under vacuum by thermal evaporation method. The cross-sectional SEM image of the device is shown in Figure 1. The device comprised of a 50 nm compact $TiO_2$ layer, a 350 nm $CH_3NH_3PbI_3$, a 260 nm spiro-OMeTAD and 80 nm Au metal back contact (Figure 1). Photovoltaic characterization of the device was done by taking I-V curves under AM1.5G (100 mW $cm^{-2}$) solar irradiation, measured by a reverse scan from +1.2 V to -0.05V and forward scan (from -0.05 to +1.2V), active area 0.0314 $cm^{-2}$. I-V curves (Figure 2) of the cell showed large hysteresis. Table 1 lists the photovoltaic parameters of the cell; reverse scan PCE of 18.0%, $J_{sc}$=24.0 mA $cm^{-2}$, $V_{oc}$= 1.034 V and FF=0.73, forward scan PCE of 8.8%, $J_{sc}$=23.9 mA $cm^{-2}$, $V_{oc}$=0.852 V and FF=0.43.

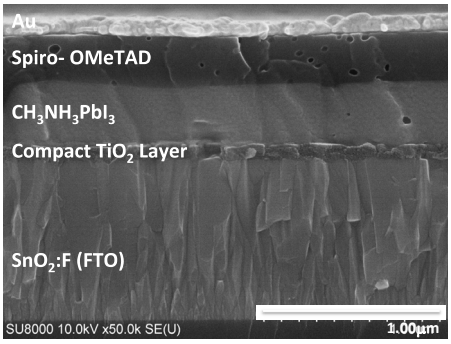


**Figure 1.** Cross-sectional SEM image of perovskite solar cells deposited on flat FTO substrate.

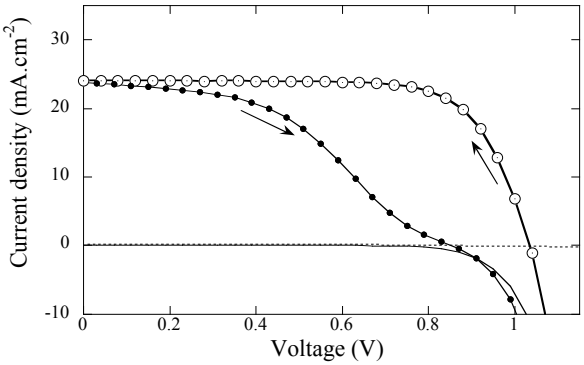


**Figure 2.** I-V curves for photovoltaic device based on planar structure perovskite solar cells measured at different scan directions (black dots forward scan, circle for reverse scan) under AM 1.5G (100 mW cm$^{-2}$).

**Table 1.** Photovoltaic parameters extracted from I-V curves for the best planar structure perovskite solar cell.

| Scan directions | $J_{sc}$/ mA cm$^{-2}$ | $V_{oc}$/V | FF | PCE/% |
|---|---|---|---|---|
| reverse | 24.0 | 1.034 | 0.73 | 18.0 |
| forward | 23.9 | 0.852 | 0.43 | 8.8 |

In order to validate hysteresis in I-V characteristics we considered several equivalent circuit models and obtained I-V curves by simulation using MultiSim Electronic Workbench application (from National Instruments). The widely used equivalent circuit of a solar cell comprises a diode, a series resistance (Rs) and shunt resistance (Rsh) (Figure S1). The series resistance (Rs) represents the total resistance of the device while the shunt resistance (Rsh) represents the resistance to leakage current. The above standard equivalent circuit was built on the Multisim's onscreen circuit board. In this simulation we used modulation power source as shown V1 in the Figure S1, Figure S2 and Figure 3. The voltage V2 shown in the Figure S1 controls the frequency of triangle wave which represents the scan speed of I-V curves. The voltage was linearly sweeped with triangle wave as shown in Figure S3 to simulate reverse scan and forward scan. To plot I-V curves across the simulated cell was monitored onscreen oscilloscope provided in the software. Two input channels are assigned; A for measured voltage at both ends of dummy resistance R3 to evaluate the current and B for voltage.

Initially Rs and Rsh values were set to calculate series and shunt resistance of the experimental I-V curve for reverse scan. Experimental I-V curve was successfully simulated with Rs = 3.8 Ω cm$^2$ and Rsh = 900 Ω cm$^2$ by confirming accuracy of the model simulation method. As shown in Figure S1, the simulated I-V curves did not change with the scan directions. This confirmed that the standard equivalent circuit having single diode with a series and a shunt resistance does not hold good I-V simulation showing hysteresis. Then, taking the carrier accumulation into account, we incorporated a capacitor in parallel to Rsh in the equivalent circuit (Figure S2). However, adding a capacitor to the standard equivalent circuit also did not simulate the experimental hysteretic I-V curves (Figure S2). Finally, we tested an equivalent circuit model (Figure 3) composed of two diodes connected in series, two capacitors, two shunt resistances (Rsh), single series resistance (Rs) and two current sources.

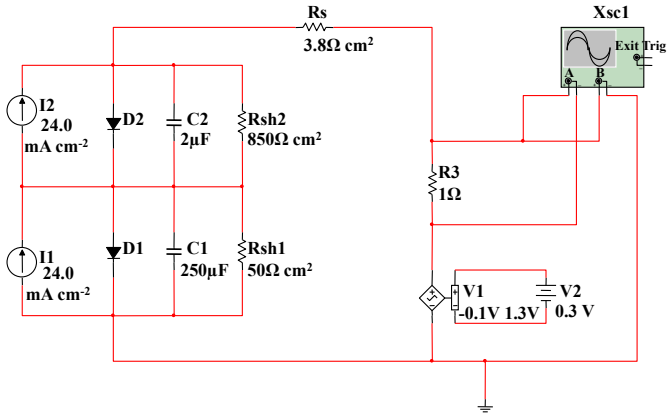


**Figure 3.** Equivalent circuit model of perovskite solar cell with double diodes, capacitances, Rsh and single Rs.

The fitting parameters of the circuit model for the simulated I-V curves are summarized in Table S1. For this model, fitting parameters (Rs, Rsh1, Rsh2,) were chosen by using calculated series and shunt resistance values from experimental I-V data (Figure 2). Initial C1 and C2 were randomly selected. Then parameters were optimized (by trial and error method) to minimize deviation between simulated and experimental curves.

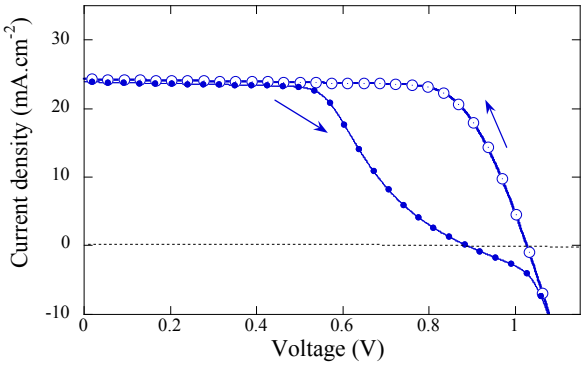


**Figure 4.** Simulated I-V curves with hysteresis using double diodes, capacitors, Rsh and single Rs model for perovskite solar cell. The extracted photovoltaic characteristics are shown in Figure S1.

As shown in Figure 4, the simulated I-V curves of this double diode equivalent circuit showed hysteresis, matching closely with the experimental I-V curves. According to this

equivalent circuit model, perovskite solar cells may consist of two active junctions with drastically different capacitances developed from carrier accumulation at the interfaces. $CH_3NH_3PbI_3$ layer is sandwiched between n- and p- type contacts and formed two interfaces. It has been already reported that $CH_3NH_3PbI_3$ forms two active junctions, one with the n-type $TiO_2$ and the other with p-type spiro-OMeTAD.[20] The interface between $TiO_2$ and $CH_3NH_3PbI_3$ shows huge lattice mismatch.[15] These mismatch produce high electrical capacitance at the interface. On the other hand, the interface between spiro-OMeTAD/$CH_3NH_3PbI_3$ layer having less mismatch creates a relatively smaller capacitive component at the interface. Hence, in the equivalent circuit model, we attribute the first part comprising diode (D2), large capacitor (C2) and shunt resistance (Rsh2) to the $TiO_2$/$CH_3NH_3PbI_3$ interface. The second part with diode (D1), single smaller capacitance (C1) and shunt resistance (Rsh1) can be attributed to $CH_3NH_3PbI_3$/spiro-OMeTAD interface.

In conclusion, we clarified the origin of hysteresis in I-V curves of a planar perovskite cell using different equivalent circuit models and simulation of their I-V curves. A planar cell showing huge hysteresis, PCE of 18.0% on reverse and 8.8% on forward scan, were used for validating the equivalent circuits. We found that the standard equivalent circuit with a diode, a series resistance and a shunt resistance does not reproduced the hysteresis of I-V curves. Even for the incorporation of a capacitive component in the circuit, the model also did not match the experimental I-V curves. However, an equivalent circuit model composed of two series connected diodes, two capacitors, two shunt resistances and a series resistance reproduced the hysteresis of the experimental I-V curves. This result suggests that the perovskite cell has two active interfaces; $TiO_2$/ $CH_3NH_3PbI_3$ and $CH_3NH_3PbI_3$/spiro-OMeTAD. The hysteresis is essentially caused by carrier accumulation at these active interfaces. We believe that the lattice mismatch or voids present at the interface $TiO_2$/$CH_3NH_3PbI_3$ create high electrical capacitance and the other interface with less defects exhibit low capacitance where the hysteresis was good agreement with the simulation.

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